REMARKS

This amendment is in response to the Final Office Action dated mailed April 4, 2006. Reconsideration of the above-identified application in view of the amendments above and the following remarks is respectfully requested.

Claims 1- 46 are currently pending in the application. Claims 1-3, 5-18, 20-35, and 37-46 have been rejected. Claims 4, 19 and 36 are objected to. Claims 1, 16 and 33 are amended herein. Claim 19 is hereby canceled. New claims 55-57 are hereby added.

Claims Rejections Under 35 USC 102(b) – Daniele et al. (US 5,412,599)

Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Daniele et al. (US 5,412,599). The Examiner's rejections are respectfully traversed.

Claim 1 defines a logic circuit which is based upon two complementary transistor networks which connect to logic inputs and outputs as defined by claim 1. The logic circuit is able to implement a wide variety of logic functions, simply by varying the structure of the internal transistor networks. Fig. 1 illustrates such a logic circuit, which is formed from two transistor networks, and having the necessary interconnections between the transistor networks and the logic inputs/outputs.

In contrast, Daniele's EEPROM cell is formed from two transistors only. In the description of Fig. 8 (col. 6 lines 17-19) Daniele states:

> ..the isolated gate I is provided with another projection 30 extending over a fourth active area 12 which has been provided with a conductivity of opposite type in respect to the type of conductivity of the active area 24. By forming the

respective source and drain diffusions, *two distinct and complementary read transistors...are formed..*

A two-transistor EEPROM cell formed from transistors T1 and T2 is likewise shown in both Figs. 17 and 18. None of these implementations forms a cell from transistor networks. (Note that transistor T3 of Figs. 17-18 has separate diffusion inputs from those of transistor T1, and therefore transistors T1 and T3 cannot be said to form a transistor network.)

In order to overcome the rejections of the Examiner and to expedite prosecution, Applicant has chosen to amend independent claims 1 and 33 to explicitly define a logic network as being formed from multiple transistors. For example, amended claim 1 now reads:

1. A complementary logic circuit, comprising:
a first logic input;
a second logic input;
a first dedicated logic terminal;
a second dedicated logic terminal;
a first logic block comprising:
a p-type transistor network for implementing a predetermined logic function, *said network comprising a plurality of p-type transistors*, and having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,
said outer diffusion connection of said p-type transistor network being connected to said first dedicated logic terminal, and said first network gate connection of said p-type transistor network being connected to said first logic input; and
a second logic block comprising:
an n-type transistor network implementing logic function complementary to said predetermined logic function, *said network comprising a plurality of n-type transistors*, and having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,
said outer diffusion connection of said n-type transistor network being connected to said second dedicated logic terminal, and said first network gate connection of said n-type transistor network being connected to said second logic input;

said inner diffusion connections of said p-type transistor network and of said n-type transistor network being connected to form a common diffusion logic terminal.

Corresponding amendments are made to independent claim 33.

The Applicant believes that independent claims 1 and 33, which include multiple-transistor networks, are now clearly distinguished over Daniele.

The Applicant respectfully acknowledges the Examiner's statement that claim 19 would be allowable if rewritten in independent form including all the limitations of the base claim. Accordingly, independent claim 16 is hereby amended to include the limitation that each of the interconnected logic elements has logic terminals separately configurable to serve as a logic output. Claim 19 is consequently canceled.

The Applicant wishes to bring new independent claim 55 to the Examiner's attention. New claim 55 defines a logic element formed from a single p-type and a single n-type transistor, where the gate connections of the two transistors serve as independent logic inputs, and are not connected together to form a common logic input. Such a logic element corresponds to the GDI* cell presented in the instant specification (see Fig. 8). Note that the basic configuration of the logic circuit of Fig. 1 contains logic inputs connecting independently to a corresponding transistor network gate connections, and is not limited to a common-logic input configuration.

Such a configuration, in which the transistor gates are not connected together, is not presented by Daniele. The EEPROM cell of Fig. 8 is formed by providing "the isolated gate I ...with another projection 30 extending over a fourth active area" (Daniele col. 6 lines 12-13). The two transistors thus share a single gate, which can only serve as a

common logic input. Independent gate logic inputs are also not present in the EEPROM cells of Figs. 17 and 18, both of which have a common gate FG.

It is therefore submitted that independent claims 1, 16, 33 and 55 are both novel and inventive over the cited prior art.

It is believed that dependent claims are allowable as being dependent on allowable main claims. The specific objections against the dependent claims are therefore not responded to individually.

No new matter has been added in the course of making the present amendments.

It is believed that all of the matters raised by the Examiner are overcome, and that all of the claims are both novel and inventive.

In view of the foregoing, it is believed this application is now in condition for allowance. An early Notice of Allowance is respectfully requested.

Respectfully submitted,

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